FOCAL PLANE PROCESSOR FOR IR DETECTION

5   **FIELD OF THE INVENTION**

The present invention relates generally to IR focal plane array detectors. More specifically, the present invention is in the field of detector pixel signal readout and processing.

10   **BACKGROUND OF THE INVENTION**

Photonic detector devices respond to received photons by creating an electric effect which can be quantified and hence provide information as regards the flux of the received photons. Focal plane arrays (FPAs) of detectors are used to obtain images of objects, whereby each detector provides a pixel in

15   the image array. In the image, each pixel is provided with a unique address and a numeric value, which can further be used for manipulating the image for extracting information from the image.

Thermal Infra red (IR) FPAs are used for obtaining images in the thermal IR range. The resolution of an imaging array in the IR is limited by two

20   factors, namely noise equivalent temperature (NET) and spatial noise, of the analog chain: the focal plane processor (FPP), the external analog circuitry

and the analog to digital conversion. An external interference, such as RF interference or signals induced by the digital system may also degrade the performance. The temporal noise of the FPP can be reduced by careful design to be negligible relative to the signal noise, providing low NET values. Yet, to overcome the spatial noise, an external process of non uniformity correction (NUC) must be carried out. A "two point correction" process is generally used, assuming the analog chain to be linear and having stable offset and gain. The final results depend upon the validity of these assumptions, and the spatial resolution becomes a main restriction, limiting the dynamic range and requiring frequent calibrations. The FPP is kept at a steady temperature, e.g. at about 77°K while the external circuitry is exposed to wide temperature variations, degrading the gain and offset stability. Also, the FPP is relatively shielded against external interference, which is not the case with the external elements. In order to reach such a low temperature and keep it steady, the sensor is disposed within a cooled dewar. The dewar has electric connections installed in the walls, in order to facilitate electrical connection with external circuits.

Heat production is a matter of high importance in the design of FPPs. The efficiency of the cooling system being very low, the amount of power consumed by the circuits of the FPP at any time must also be limited. Sampling rates, sampling resolution, and output rates are factors which affect heat production. The use of components and combinations thereof having a low power consumption is favoured in the design of cooled FPPs. A trade – off between imaging parameters is a compromise often imposed for obtaining desirable image parameters. Accordingly, image frame rate at the expense of

image resolution or image size are known in the art. Continuous attempts are made by various system designers to overcome the limitations described, striving to attain a high frame rate and a high resolution, with a reasonable power dissipation.

5   The value of the electric effect associated with each detector of the FPA is converted into a digital format, before it can be subjected to digital image processing. However, there are a number of critical reasons favouring conversion to digital format at an early stage as possible of the signal corresponding to each pixel. US 5,886,659 discloses an on - focal plane analog

10   to digital conversion application. Benefits of having the analog – to –digital conversion in the focal plane are discussed in that publication, the contents of which are incorporated herewith by reference.

Integrated converters have used several types of conversion schemes. Single-slope analog to digital conversion is a well - established technique. For

15   example, US 5,742,058 discloses an analog to digital conversion in the focal plane utilizing a single slope conversion cycle. The Dual-slope conversion provides better accuracy and stability (R. Van De Plassche, cited below). Yet, both techniques require quite long conversion times, being based on counters: the full - scale time of an n-bit single-slope converter is $2^n * Tc$,

20   where Tc is the clock cycle time. The dual slope requires up to twice that time. The dual-ramp single-slope method, described by R. Van De Plassche in: INTEGRATED ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS, Kluwer Academic Press, pp. 274 – 289, 1994, the contents

of which are incorporated herein by reference, promises both high resolution and reduced conversion time.

It is on the background hitherto described, that the present invention was conceived. The invention described below provides a basis for increasing the rate of
5   sampling digitally at the FPP level, without compromising the resolution of each pixel.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is schematic description of the main structural features of an IR sensor system in which the invention is implemented;

10   Fig. 2 is a flow chart describing schematically the process of the invention;

Fig. 3A is a circuit of the invention for converting the charge of a pixel;

Fig. 3B is a charge DAC optionally used in the system of the invention;.

Fig. 3C is another charge DAC optionally used in the system of the invention;

15   Fig. 3D is another charge DAC optionally used in the system of the invention, enabling multi step conversion;

Fig. 4A is an implementation of a pixel charge converting circuit of the invention adapted for an array of pixels;

Fig. 4B is a graph describing the main wave-shape forms in the circuit of
20   Fig. 4A in the course of one conversion cycle;

Fig. 5 is a charge converting circuit with an integrator added;

Fig. 6A is a description of detailed circuitry of the invention, wherein an integrator is added and the current sources are implemented by a dual ramp generator and a capacitor;

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Fig. 6B is a description of the main wave - shape forms in the circuit of

Fig. 6A, implemented in the course of one conversion cycle;

Fig. 7. is a schematic description of the interconnections existing between

the main components of the imaging system, in accordance with the present

5   invention;

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DETAILED DESCRIPTION OF THE PRESENT INVENTION

A system of the invention is implemented in association with an integrated circuit device, a focal plane processor (FPP). The FPP is disposed within a cooled dewar, as described schematically in **Fig. 1** to which reference is now made. A longitudinal cross section elevation in an IR sensor is shown, in which the FPP **14** of the invention is functional. Metal plate **16** is adjacent cold finger **18**. The FPP is thermally connected while electrically isolated, with metal plate **16** through ceramic plate and spacers **20**. To ceramic plate and spacers **20**, which is electrically insulating, are connected wire bonds **22**. FPP chip **14** supports detector array chip **24** through indium bumps **26**, whereby for each detector in the detector array chip **24** there exists one bump connecting to the respective pixel in the FPP chip **14**. Penetrating through the envelope of the dewar **26** are connecting pins **28**. Wire bonds **22** connect pads (not shown) of FPP **14** to the appropriate connecting pins, having intermediate pads on the ceramic plate **20**. The connecting pins provide electrical contact to external circuits **30**.

The process of the invention is summarized schematically in **Fig. 2** to which reference is now made. In step **40**, photon flux is captured on a detector pixel, causing a corresponding build – up of charge in the respective FPP pixel in step **42**. In step **44** the charge in the FPP pixel is quantified digitally. In step **46** the results of the quantification are processed and in step **48** the processed data is transmitted to a programmable logic outside of the dewar for further processing. In step **50**, digital numbers are calculated and pixels are remapped to restore the image.

FPP pixel charge digital conversion

The charge accumulated in the pixel in the FPP of the invention is according to the present invention converted to a digital form by a circuit modified from Van De Plassche, cited above. The original circuit, known as a dual ramp

5 single slope converter, samples the input voltage and then converts it into a digital number. The modified circuit of the present invention is a charge converter circuit, wherein the conversion is carried out directly on the pixel capacitor and no charge - to - voltage conversion and sampling are performed. The function of the circuit of the invention is described in reference to **Fig. 3A**. Peripheral block

10 **52** contains a comparator **66**, a charge output digital–to-analog converter (DAC) **62** and of controller **64**. The input port of peripheral block **52** is line **68**, which connects between the output port of the DAC **62** and comparator **66**. Qpx, the charge to be converted, is stored in pixel capacitor **70**. Closing switch **200** connects capacitor **70** to line **68** forming a charge ADC. DAC **62** produces a

15 charge of opposite polarity, the value of which is controlled digitally by the controller **64**. The digital control value (in bits) which eliminates Qpx (as indicated by the comparator **66** output) is the conversion output. No sampling of the input charge is required as the charge is eliminated directly on the pixel capacitor. On the next conversion, another pixel capacitor **221** is connected to the same

20 peripheral block **52**, forming a "new" ADC.

The charge DAC of the invention can be implemented in several ways. Two exemplary implementations of such a charge DAC are described in **Figs. 3B** and **3C** to which reference is now made. In **Fig. 3B** a DAC implementation used in a successive approximation mode (wherein the capacitance ratios are 2:1) is

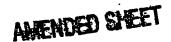25 described, in which the charge for elimination of the Qpx is provided by a set of

capacitors **72** containing capacitors C_1- C_n, injecting charge doses. It is also possible to use only the smallest capacitor, switching it many times and counting the number of switching necessary to eliminate the converted charge.

5   The DAC of Fig. **3C** is applicable in a charge conversion scheme. The charge supplied by the current source **74** is determined by the duration of its connection to the DAC OUT port **68**. The current source **74** is disconnected when the pixel capacitor charge is cancelled. The duration of the connection of source **74**, is measured digitally, producing the conversion quantitatively. In a preferred embodiment of the invention, the total time of conversion is shortened using
10   several (typically two) current sources as shown in Fig. **3D**. The required charges are obtained by switching-on a sequence of current sources for a given time, producing charge packets accordingly. Source **76** is turned on first. Each consecutive current source turned on has a significantly reduced magnitude (typical ratios may be 16 or 32). The conversion is done accordingly in several
15   steps, refining the resolution per step, as will be described later.

The "dual ramp single slope ADC" employs a quantification cycle which implements two steps. In the first step MS (most significant) part of the numeric value is determined, and in a second step, LS (least significant) part of the numeric value of the charge is determined. The two parts of the digital values of the
20   measured quantity must be combined to form a complete digital word, as will be explained later on.

Figs. **4A - B** demonstrate an embodiment of the invention, implementing a two-step conversion: Fig. **4A** shows the block diagram of the circuit, and Fig. **4B** shows the main wave-forms during the conversion cycle. At time t_1 switches S3
25   **94** and S4 **98** are closed, connecting the pixel capacitor **100** and the current

source 110 to the input 68 of comparator 92. Switch 94 remains closed throughout the conversion up to time t_7, while switch 98 opens when the pixel charge is eliminated, as indicated by the comparator. Since the output of the comparator is synchronized to the next clock pulse, switch 98 is opened at t_3

5   instead of t_2 and the voltage at the input 68 overshoots negatively, the residual voltage being proportional to $\Delta t = t_3 - t_2$. This overshoot will be eliminated in the next step: at time t_5 switch S6 112 is closed, connecting the current source 114, the magnitude of which is much smaller (e.g. 32 times) and the polarity is opposite to source 110 polarity. The charge is eliminated at time t_6, with the final

10   residual error of the conversion. The period between t_1 to t_4 is the duration of the first step, which enables the conversion of the maximal pixel charge. The period between t_5 to t_7 is the duration of the second step for a maximal $\Delta t = t_3 - t_2$. The clock is connected by switch S5 116 to the counter during two periods. First, from t_1 to t_3 for providing the "MSB count", and subsequently from t_5 to t_6 for providing

15   the "LSB count". The final count is achieve by subtracting the LSB counts from the MSB ones, while the relative weight of the two counts is determined according to the current ratio between the two current sources 110 and 114.

However, in practice, the pixels are arranged in the dense framework of a matrix of rows and columns which may be long such that certain implications are

20   inevitable trying to adapt a solitary pixel AD conversion application to a pixel array application, such as a column of the array. Accordingly, the following two concerns must be dealt with. The long column lines add mutual parasitic capacitances, the values of which may reach one order of magnitude larger then the pixel capacitor C_{px}. Consequently, during the conversion, a cross-talk exists

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between adjacent column lines due to voltage transients, impairing the function of the matrix.

In accordance with one embodiment of the present invention, an integrator, the input of which is a virtual ground, is added as a first stage of the comparator of the charge ADC circuit. This architectural feature helps to overcome the above mentioned problem as the column line in this configuration becomes connected to a virtual ground. Such a configuration is described in **Fig. 5** to which reference is now made. Integrator **120**, is disposed between the comparator **122** and the column line **124**, The charge to be converted is stored in the pixel capacitor **126**, whereas the charge injected from DAC **128** into the column line **124**, eliminates this charge as described above.

The two current sources **110** and **114** of **Fig. 4A** to which reference is again made, can be produced by a dual voltage ramp generator, driving a capacitor as will be described next. A configuration, combining the above mentioned integrator and the dulal ramp generator driving a capacitor is described in **Fig. 6A** and **6B** to which reference is now made. In **Fig. 6A** is shown an AD Conversion circuit in accordance with a preferred embodiment of the invention, the function of which is explained with reference to the conversion cycle and switching sequences described in **Fig. 6B**. In **Fig. 6A** Integrator **190**, is disposed between the comparator **192** and the column line **68**. The two above mentioned current sources are implemented by ramp generator **194** and capacitor C1 **196**. At time t_0 the quiescent output voltage of integrator **190**, is forced by closing momentarily switch S1 **198** to Vpch, (pre - charge voltage), which is also the reference voltage for comparator **192**. Closing switches S3 **200**, S4 **202** and S5

204 at time t_1, the conversion of the charge of a pixel, accumulated in capacitor Cpxl **206** begins. First, the output voltage of integrator **190** is lowered. Closing switch **S4 202** at time t_1, a constant current source is established by the combination of a linear ramp voltage (ramp **204** of **Fig. 6B**) and the capacitor C1

5   **196**, eliminating the measured charge while the integrator output goes up linearly. Switch **206** closes simultaneously with switch **202**. Counter **208**, which was reset earlier, starts counting the clock pulses. Reaching Vpch at time t_2, the integrator activates the comparator. The period $t_2 - t_1$ is a true indication of the signal to be measured. Yet, the output of the comparator is synchronized to the

10   next clock, and only then, at t_3 it opens switch **202** and samples the counter reading (switch **206** remains closed until time t_4 in order to serve other ADCs). As a result, the output of the integrator continues to rise for a period Δt (see **Fig. 6B**), so that the counter reading provides only the MS count, and a value, proportional to Δt should be subtracted with higher resolution. This is done by

15   writing the count (considered to be the MS bits) to latches, resetting counter **208** and closing again switch **206** and switch **202** at time t_5, which connects a second ramp (ramp **210** in **Fig. 6B**), the slope of which is positive and slower. The output of the integrator goes down and reaches Vpch at time t_6, disabling the comparator. The period between t_1 to t_4 is the duration of the first ramp, which

20   enables the conversion of the maximal pixel charge. The period between t_5 to t_7 is the duration of the second ramp for a maximal Δt. Switch S7 **160** must be closed whenever there is no ramp, in order to provide the initial conditions for capacitor C1 **196**. The counter reading is sampled at time t_6, providing the LS count to be subtracted (with the proper weight) from the digital number

represented by the former MS bits. The ratio between the absolute values of the slopes of the two ramps determines the number and weight of LS bits. The value of Δt is nominally less then one clock time. Yet, in practice, due to delays in the comparator and the switching, it might reach as high as some clock times, the actual number of which depends also upon the clock frequency. Consequently, the period and the number of counter stages assigned to the second ramp is to be increased accordingly.

The combination of the common linear voltage ramps (**204** and **210** in **Fig. 6B**) driving simultaneously the capacitors **196** (in **Fig. 6A**) in the peripheral blocks of all columns, enables applying low level DC current sources of approximately the same amplitude to all the ADCs. Thus the use of current mirrors, which are not accurate enough (especially in the nano-ampere levels), is avoided. The ramp generator **194** (in **Fig. 6A**) is basically an integrator, fed at each step of the conversion cycle by a constant current source of appropriate amplitude and polarity.

In order to decrease the readout time of a large matrix, two or more peripheral blocks can be implemented per column, provided that the number of column lines is increased accordingly, wherein each column line connects part of the pixels of the column to a different peripheral block. All the peripheral blocks operate simultaneously, thus the charges of the pixels in two or more rows of the matrix are converted at a time.

In order to further decrease the conversion time without loosing resolution, the "dual ramp single slope AD Convertion" concept can be further extended into a multi ramp AD Convertion, where additional conversion steps, having

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successively decreased weights, are employed. This may be desirable in the case of very high resolution converters.

Programmable logic applications in the present invention

5   The FPP of the present invention is applicable to IR imagers in general. Yet, it is especially advantageous in cooled imagers, where the heat dissipated in the focal plane should be removed by cooling to a low and stable temperature. Therefore, architectural and functional considerations of the make-up of the integrated circuit have been made in order to decrease the power dissipation in

10   the FPP integrated circuit. In accordance with one aspect of the invention, a programmable logic device, external to the dewar in which the integrated circuit of the sensor is disposed, performs several tasks. The first one relates to the digital functions of the AD Conversions which are partially performed outside of the dewar. These functions being performed in the uncooled environment, serve

15   to decrease the amount of components and heat dissipation in the FPP, therefore potentially improving the overall performance of the imager. As explained above, the digital value of each pixel is obtained in a MS part and an LS part. The two parts, after initial processing in the FPP, are finally combined to form one digital word in the external programmable logic device. The second

20   task relates to the remapping of the pixels. The data transmission from the FPP to the programmable logic is optimized to minimize focal plane power dissipation. Consequently, the bits of a digital word transmitted from the dewar include a mixture of data from two pixels. Such mixed data is remapped in the external logic device, to restore the image.

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The external programmable logic device also adds flexibility and optimizes the conversion cycle. Whereas the order of succession of the various conversion steps is fixed, the duration of each step is controlled externally. Thus, the duration of each step is set as required by the actual performance sequence,

5   avoiding the need to reserve lengthy intervals of time for confidence margins. The data transfer associated with this aspect of the invention is described with reference to **Fig. 7**. The detector assembly **270**, includes a focal plane module **272** and an external proximity board **274**. The proximity board is a printed circuit board, placed close to the dewar pins, upon which the programmable logic such

10   as FPGA (field programmable gate array) **276**, a clock generator **278** and power supply regulation circuits **280** are mounted. In the focal plane module **272**, the detector component **282** and the FPP **284** are included. The interconnections between the proximity board **274** and the focal plane module **272** are divided into four groups: regulated FPP power supplies bus, slow communications link, FPP

15   clock and timing link and the raw data bus.

Through the conventional comparatively slow communication bus, various operation parameters of the FPP, which are not directly involved in the timing of the analog-to-digital conversion steps, are controlled, These include, inter alia, "integrate-then-read" (ITR) or "integrate-while-read" (IWR) modes of operation,

20   working points, readout window size and location, etc. One parameter should be mentioned here, namely the resolution of the analog-to-digital conversion. The duration of a conversion cycle depends also on the resolution, increasing with the resolution. Some bits of the slow communication stream control the resolution, through the ratio between the slopes of the ramps **204** and **210** (in

25   **Fig. 6B**), enabling a trade-off between the resolution and the frame-rate.

A faster link carries to the FPP the clock signal and the timing information of the conversion steps, mentioned earlier. In this fast channel, a stream of short pulses is sent on a wire from the external programmable logic to the FPP, where each pulse is recognized in the FPP as the start or end of a specific step.

5 Programming the intervals between the pulses, the optimal conversion duration is determined. The raw data bus carries the partially processed data produced by the ADCs, from the FPP to be finally processed and remapped in the programmable logic device.

10 A different aspect of the imaging array which relates to the external programmable logic, is its exploitation as a user interface. Thus, in some embodiments of the invention, the programmable logic device can be used also as an interface to the external system **290** in **Fig. 7**, simplifying the users' interaction with the FPP. While the FPP of the invention operates with the

15 optimal clock and timing for the conversion, the user can approach the buffered output on the programmable logic implementing specific communications protocol and clock. The clock of the user system is independent of the clock of the detector assembly, and does not have to be synchronized with it. The dialog between the two systems can then be established by an handshaking

20 implemented on the programmable logic device.

As described so far, the system of the invention is most beneficial in cooled FPPs, typically implemented in thermal IR imaging. It is nevertheless contended that the same system can be used in any FPP systems, for other imaging purposes, such as visible, near infra - red and X – ray. In such systems,

heat dissipation in the FPP may be less critical, but the benefits of the system

are still evident.